REMARKS

Claims 1-8 were pending in the application. Claims 1 – 4 and 8 are being presently amended. Claim 5 - 7 are being cancelled. Claims 9 and 10 are being newly added. Amendments to claims 1 and 2 are based on the language of the specification page 5, line 6, to page 7, line 5, and Fig. 1. The language of the new claim 9 and 10 is based on the language of claim 1 as originally filed and Fig. 1.

Priority under 35 U.S.C. § 119

Applicant notes with appreciation that the Examiner acknowledged a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f) to Polish Patent Application No. P-354827 filed on July 1, 2002 and confirmed that all certified copies of the priority documents have been received.

All outstanding requirements will now be addressed in the order they appear in the Office Action mailed May 18, 2007.

Rejections under 35 USC § 103

1-7. Claims 1 - 8 stand rejected under 35 U.S.C. 103 as being allegedly unpatentable over Huang (United States Patent No. 4,627,060). Specifically, the Office Action alleges that Huang discloses a circuit for detection of external microprocessor watchdog device execution, which includes all limitations as claimed in claims 1-8.

Applicant respectfully submits that the object of the present invention is to detect the execution of an internal watchdog device in a microprocessor, in which the internal watchdog device signal line is not available from outside the microprocessor.
This problem is not addressed by Huang because, as acknowledged by the Examiner, Huang refers to a watchdog device disposed *externally* to the microprocessor. The "system reset"

(80) and "watchdog fired" (86) signals are available outside the watchdog timer (10) and can be connected to other devices of the microprocessor system in which the circuit proposed by Huang could be user.

In contrast, the present invention teaches a watchdog device *internal* to the microprocessor, where the signal about watchdog execution is not available from the outside. In order to detect the execution of the internal watchdog device, a separate input/output line (11) of the microprocessor is configured to transmit information about the microprocessor reset. This input/output line (11) transmits information about the microprocessor reset independently from the reset signal (3) generated by the watchdog device. The input/output line (11) is connected to a device for resetting the microprocessor system via a flip-flop (12), such that a microprocessor reset detected on the input/output line (11) causes the device (19) to generate a system reset signal. Such solution is not taught by Huang.

CONCLUSION

In view of the foregoing amendments and remarks, Applicant submits that the pending claims are in condition for allowance. Early and favorable reconsideration is respectfully solicited. Should an extension of time be required, Applicant hereby petitions for same and request that the extension fee and any other fee required for timely consideration of this submission be charged to **Deposit Account No. 503182**.

Customer Number: **33,794**

Respectfully Submitted,

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